

# PDP11

TEST 14 TRAPS TEST  
MD-11-DZKAR-A

EP-DZKAR-A-DI-A  
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FICHE 1 OF 1

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**digital**  
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This microfiche card contains a grid of frames. The first column on the left contains 14 frames, each with a header and a table of data. The remaining frames in the grid contain various data points, likely representing trap test results for different traps or conditions. The data is organized in a structured, tabular format.



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1. ABSTRACT

THIS IS A TEST OF ALL OPERATION AND INSTRUCTION THAT CAUSE TRAPS. ALSO TESTED ARE TRAP OVERFLOW CONDITIONS, ODDITIES OF REGISTER 6, INTERRUPTS AND THE RESET INSTRUCTIONS.

THIS PROGRAM HAS BEEN RENAMED FROM DON TO DZKAR.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11/20, 11/05 STANDARD COMPUTER

2.2 STORAGE

2.2.1 PROGRAM STORAGE - THE ROUTINE USES MEMORY FROM 0000 TO 17500.

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL ABSOLUTE TAPES SHOULD BE FOLLOWED:

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTING

THE PROGRAM STARTS AND RESTARTS AT 200 FOR A 4K SYSTEM

4.2 STARTING ADDRESS OR ADDRESSES

(A) 200 = STARTING ADDRESS FOR 4K  
202 = STARTING ADDRESS FOR 8K

204 = STARTING ADDRESS FOR 12K  
 206 = STARTING ADDRESS FOR 16K  
 210 = STARTING ADDRESS FOR 20K  
 212 = STARTING ADDRESS FOR 24K  
 214 = STARTING ADDRESS FOR 28K

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4.3 PROGRAM AND/OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY. (BOTTOM 4K)  
 SET SWITCH REGISTER TO STARTING ADDRESS,  
 LOAD ADDRESS,  
 PRESS START,  
 THE PROGRAM WILL LOOP,  
 AND RING A BELL AFTER EACH ITERATIONS

5. OPERATION PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

NO SWITCHES ARE USED

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200

5.2.2 SCOPE

IS A "MOV %7,%0" THAT IS PLACED BETWEEN EACH SUBTEST  
 IN THE INSTRUCTION SECTION. IF A SCOPE LOOP IS  
 NEEDED. INSERT A BRANCH TO THE PREVIOUS SCOPE  
 LOCATION AT THE CURRENT SCOPE LOCATION.

5.2.3 HLT

INDICATES THE UNIQUE ADDRESS THAT TAGS THE FAILING  
 SUBTEST. THE INCORRECT DATA AT THE TIME OF THE  
 FAILURE MAY OR MAY NOT BE DISPLAYED IN  
 REGISTER ZERO, WHICH IS THE DATA REGISTER ON  
 A HALT.

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2065.2.4 TRAPCATCHER  
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THIS IS A SERIES OF INSTRUCTIONS DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS, THAT OCCUR IN THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

THE PRINCIPAL OF THIS ROUTINE IS: THE VECTOR ENTRANCE ADDRESS POINTS TO THE NEXT SEQUENTIAL WORD WHICH WILL CONTAIN A HALT (00000) (THIS LOCATION IS ALSO THE STATUS WORD FOR THAT VECTOR ENTRANCE. BUT THIS WILL HAVE NO EFFECT ON IT ALSO BEING THE NEXT INSTRUCTION).

IF A HALT OCCURS IN THE TRAP OR INTERRUPT VECTOR AREA, REGISTER SIX SHOULD BE EXAMINED TO DETERMINE ITS CONTENTS, THEN USE REGISTER SIX CONTENTS AS AN ADDRESS TO DETERMINE THE LOCATION THE PROGRAM WAS AT, WHEN THE INTERRUPT OR TRAP OCCURRED. (MEMORY AS SPECIFIED BY R6 CONTAINS THE PC OF THE INSTRUCTION FOLLOWING THE INSTRUCTION WHERE THE TRAP OCCURRED).

## 5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 LOADING AND STARTING AT 200 STARTS THE TEST IF AN ERROR IS DETECTED. THERE WILL BE A HALT. WHEN A HALT OCCURS AND IT IS NECESSARY TO SCOPE ON IT, PLACE INSERT A BRANCH INSTRUCTION IN THE SCOPE LOCATION FOLLOWING THE HALT. THE BRANCH INSTRUCTION SHOULD BRANCH YOU TO THE PREVIOUS SCOPE LOCATION.

## 6. ERRORS

6.1 ALL ERRORS WILL CAUSE A HALT.

## 6.2 ERROR RECOVERY

ON TRAP ERRORS - RESTART AT STARTING ADDRESS DEPRESS CONTINUE TO CONTINUE TEST

## 7. RESTRICTIONS

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## 7.1 STARTING RESTRICTION

NONE

## 7.2 OPERATIONAL RESTRICTION

NONE

## 8. MISCELLANEOUS

## 8.1 EXECUTION TIME

FOR THE TEST ABOUT 45 SECONDS

## 9. PROGRAM DESCRIPTION

THIS PROGRAM CHECKS THAT ON ALL TRAP OPERATIONS REGISTER 6 IS DECREMENTED THE CORRECT AMOUNT, THAT THE CORRECT PC IS SAVED ON THE STACK, THAT THE OLD CONDITION CODES AND PRIORITY ARE PLACED ON THE STACK AND THAT THE NEW STATUS AND CONDITION CODES ARE CORRECT. BOTH THE "TRAP" AND "EMT" TRAP INSTRUCTIONS ARE TESTED THAT ALL COMBINATION WILL TRAP. CHECKED ALSO IS THAT ALL RESTRICTED INSTRUCTIONS WILL TRAP. VERIFICATION OF THE "TRT" INSTRUCTION (00003) WHICH IS USED FOR SOFTWARE DEBUG ROUTINES: ODT, DDT. ALSO THERE IS INCLUDED OF A SPECIAL REGISTER TEST TO SEE IF ANY AUTO DECREMENT OF REGISTER WILL CAUSE A TRAP OVERFLOW WHEN REGISTER 6 IS LESS THAN 400. TRAP OVERFLOW SHOULD ALSO OCCUR WITH TRAPS AND INTERRUPTS WHEN REGISTER 6 IS LESS THAN 400. SPECIAL CHECKS ARE MADE TO SEE IF BUS ERROR TRAPS OCCUR ON ODD ADDRESS WITH WORD INSTRUCTION AND NON EXISTENT MEMORY.

## 10. LISTING

## 11. FLOW CHART(S)

.ENDR

261			: TEST 14	
262			: COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.	
263			: PDP-11 TRAP INSTRUCTION TEST AND ODD ON UNIQUE R6 OPERATIONS	
264			: ALL INSTRUCTIONS THAT ARE RESERVED	
265			: SHOULD TRAP TO LOCATION 10, AND THE	
266			: PC THAT POINTS TO THE TRAPPING INSTRUCTION	
267			: SHOULD BE PLACED ON THE STACK	
268				
269	000006		LP=%6	
270	000000		TAB=%0	
271	000001		LAST=%1	
272	000002		FIRST=%2	
273	010700		SCOPE=010700	; MOV REGISTER 7 TO REGISTER ZERO TO TAG LAST TEST
274	000000		HLT=HALT	
275	000003		TRT=3	
276	000004		ITRAP5=4	
277	000004		RTRAP5=4	; RESERVED INST AND ILLEGAL ADDRESSES
278	000014		RTRAP4=14	; FOR TRACE TRAP
279	000030		RTRAP3=30	; FOR EMULATOR TRAP
280	000020		RTRAP2=20	; FOR IOT TRAP
281	000034		RTRAP1=34	; FOR TRAP INST
282	177564		TTCSR=177564	
283	177560		TRCSR=177560	
284	000240		BELL=240	
285	000240		NOP=240	
286	177776		STATUS=177776	
287	070000		TRAPA=70000	
288	000010		RTRAP=10	
289	004700		ILLA=004700	
290	000100		ILLB=100	
291	177776		CC=177776	
292	000000		. = 0	
293			. REPT 40	
294			. +2	
295			HALT	; TRAPPED TO PREVIOUS ADDRESS
296			. ENDR	
297	000000	000002	. +2	
298	000002	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
299	000004	000006	. +2	
300	000006	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
301	000010	000012	. +2	
302	000012	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
303	000014	000016	. +2	
304	000016	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
305	000020	000022	. +2	
306	000022	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
307	000024	000026	. +2	
308	000026	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
309	000030	000032	. +2	
310	000032	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
311	000034	000036	. +2	
312	000036	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
313	000040	000042	. +2	
314	000042	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
315	000044	000046	. +2	
316	000046	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS

317	000050	000052	.+2	
318	000052	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
319	000054	000056	.+2	
320	000056	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
321	000060	000062	.+2	
322	000062	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
323	000064	000066	.+2	
324	000066	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
325	000070	000072	.+2	
326	000072	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
327	000074	000076	.+2	
328	000076	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
329	000100	000102	.+2	
330	000102	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
331	000104	000106	.+2	
332	000106	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
333	000110	000112	.+2	
334	000112	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
335	000114	000116	.+2	
336	000116	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
337	000120	000122	.+2	
338	000122	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
339	000124	000126	.+2	
340	000126	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
341	000130	000132	.+2	
342	000132	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
343	000134	000136	.+2	
344	000136	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
345	000140	000142	.+2	
346	000142	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
347	000144	000146	.+2	
348	000146	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
349	000150	000152	.+2	
350	000152	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
351	000154	000156	.+2	
352	000156	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
353	000160	000162	.+2	
354	000162	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
355	000164	000166	.+2	
356	000166	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
357	000170	000172	.+2	
358	000172	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
359	000174	000176	.+2	
360	000176	000000	HALT	; TRAPPED TO PREVIOUS ADDRESS
361				
362		000046	.=46	
363	000046	007612	SENDAD	
364				
365		000052	.=52	
366	000052	040000	40000	
367				
368				
369		000200	.=200	
370				
371	000200	000410	BR	ST4K ;14K
372	000202	000425	BR	ST8K ;18K



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373 000204 000431 BK ST12K ;12K
374 000206 000435 BR ST16K ;16K
375 000210 000441 BR ST20K ;20K
376 000212 000445 BR ST24K ;24K
377 000214 000451 BR ST28K ;28K
378 000216 000167 004224 JMP TONT ;ERROR ON ERROR
379 000222 005767 177614 ST4K: TST 42 ;WITH ACT11 OR DDP1
380 000226 001406 BEQ .+16
381 000230 012767 000240 006022 MOV #NOP,AUTO
382 000236 012767 000240 006024 MOV #NOP,AUTO1
383 000244 012767 020000 005756 MOV #20000,CORH
384 000252 000167 000122 JMP BEGIN
385 000256 012767 040000 005744 ST8K: MOV #40000,CORH
386 000264 000167 000110 JMP BEGIN
387 000270 012767 060000 005732 ST12K: MOV #60000,CORH
388 000276 000167 000076 JMP BEGIN
389 000302 012767 100000 005720 ST16K: MOV #100000,CORH
390 000310 000167 000064 JMP BEGIN
391 000314 012767 120000 005706 ST20K: MOV #120000,CORH
392 000322 000167 000052 JMP BEGIN
393 000326 016767 137446 005674 ST24K: MOV 140000,CORH
394 000334 000167 000040 JMP BEGIN
395 000340 012767 160000 005662 ST28K: MOV #160000,CORH
396 000346 000167 000026 JMP BEGIN
397 000400 000400 . =400
398
399 ;TEST THAT A TRAP OCCURS ON ALL RESTRICTED INSTRUCTION
400 000400 010700 BEGIN: SCOPE
401 000402 012706 010050 MOV #BUFF,LP ;LINK POINTER SETUP
402 000406 012767 000420 177374 MOV #RETA,RTRAP ;RETURN LOCATION
403 000414 070000 TRAPA ;RESERVED INSTRUCTION, SHOULD TRAP
404 000416 000000 HLT
405 000420 010700 RETA: SCOPE
406 ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
407 000422 012706 010050 MOV #BUFF,LP ;LINK POINTER SETUP
408 000426 012767 000436 177354 MOV #RETB,RTRAP ;RETURN POINTER
409 000434 070000 TRAPA ;RESERVED INSTRUCTION
410 000436 020627 010044 RETB: CMP LP,#BUFF-4 ;TEST DECREMENT OF LP
411 000442 001401 BEQ .+4
412 000444 000000 HLT ;NOT DECREMENTED TWO WORDS
413 000446 010700 SCOPE
414 ;TEST THAT PROPER P.C. IS SAVED
415 000450 012706 010050 MOV #BUFF,LP ;LINK POINTER SETUP
416 000454 012767 000464 177326 MOV #RETC,RTRAP ;RETURN FROM TRAP POINTER
417 000462 070000 TRAPA ;TRAP ON THIS INSTRUCTION
418 000464 022767 000464 007352 INSTC: RETC: CMP #.,BUFF-4 ;CHECK FOR INCREMENTED P.C.
419 000472 001401 BEQ .+4
420 000474 000000 HLT ;INCORRECT P.C.
421 000476 010700 SCOPE
422 ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
423 000500 010700 SCOPE
424 000502 012706 010050 MOV #BUFF,LP ;SET UP
425 000506 012767 000524 177274 MOV #RETD,RTRAP ;SET UP
426 000514 005067 177256 CLR CC ;CLEAR CC AND PRIORITY
427 000520 000257 CCC
428 000522 070000 TRAPA ;TRAP
  
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429	000524	026727	007316	000000	RETD:	CMP	BUFF-2, #0	; TEST THAT OLD STATUS WENT TO STACK
430	000532	001401				BEQ	.+4	; TEST FOR ALL ZEROS
431	000534	000000				HLT		; INCORRECT STATUS
432	000536	010700				SCOPE		
433	000540	012706	010050			MOV	#BUFF, LP	; SET UP
434	000544	012767	000564	177236		MOV	#RETE, RTRAP	; SET UP
435	000552	012767	000357	177216		MOV	#357, CC	; SET PRIORITY
436	000560	000277				SCC		; SET CC
437	000562	070000				TRAPA		; TRAP
438	000564	026727	007256	000357	RETE:	CMP	BUFF-2, #357	; COMPARES STATUS ON STACK
439	000572	001401				BEQ	.+4	; TEST FOR ALL ONES
440	000574	000000				HLT		; INCORRECT STATUS ON STACK
441	000576	010700				SCOPE		
442								; TEST THAT "NEW" STATUS IS CORRECT
443	000600	012706	010050			MOV	#BUFF, LP	
444	000604	012767	000620	177176		MOV	#RETF, RTRAP	
445	000612	005067	177174			CLR	RTRAP+2	; CLEAR FUTURE PRIORITY AND CC
446	000616	070000				TRAPA		
447	000620	100001			RETF:	BPL	.+4	; TEST FOR "C" CLEARED
448	000622	000000				HLT		; C NOT CLEARED
449	000624	001001				BNE	.+4	
450	000626	000000				HLT		; Z NOT CLEARED
451	000630	102001				BVC	.+4	
452	000632	000000				HLT		; V NOT CLEARED
453	000634	103001				BCC	.+4	
454	000636	000000				HLT		; C NOT CLEARED
455	000640	032767	000340	177130		BIT	#340, CC	; TEST PRIORITY
456	000646	001401				BEQ	.+4	
457	000650	000000				HLT		; PRIORITY NOT ZERO
458	000652	010700				SCOPE		
459	000654	012706	010050			MOV	#BUFF, LP	
460	000660	012767	000576	177122		MOV	#RETG, RTRAP	
461	000666	012767	000357	177116		MOV	#357, RTRAP+2	; SET NEW "CC" AND PRIORITY
462	000674	070000				TRAPA		; TRAP HERE
463	000676	100401			RETG:	BMI	.+4	
464	000700	000000				HLT		; N NOT SET
465	000702	001401				BEQ	.+4	
466	000704	000000				HLT		; Z NOT SET
467	000706	102401				BVS	.+4	
468	000710	000000				HLT		; V NOT SET
469	000712	103401				BCS	.+4	
470	000714	000000				HLT		; C NOT SET
471	000716	016706	177054			MOV	CC, LP	
472	000722	042706	000017			BIC	#17, LP	
473	000726	022706	000340			CMP	#340, LP	
474	000732	001401				BEQ	.+4	
475	000734	000000				HLT		; PRIORITY WAS CHANGED
476	000736	010700				SCOPE		
477	000740	012767	000012	177042		MOV	#12, 10	
478	000746	005067	177040			CLR	12	
479								; TEST THAT A TRAP OCCURS FOR A "TRAP" INSTRUCTION
480	000752	010700				SCOPE		
481	000754	012706	010050			MOV	#BUFF, LP	; LINK POINTER SETUP
482	000760	012767	000772	177046		MOV	#RETA1, RTRAP1	; RETURN LOCATION
483	000766	104400				TRAP		; RESERVED INSTRUCTION, SHOULD TRAP
484	000770	000000				HLT		

# K01

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485 000772 010700          RETA1:  SCOPE
486          ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
487 000774 012706 010050          MOV      #BUFF,LP          ;LINK POINTER SETUP
488 001000 012767 001010 177026  MOV      #RETB1,RTRAP1    ;RETURN POINTER
489 001006 104400          TRAP                      ;RESERVED INSTRUCTION
490 001010 020627 010044          RETB1:  CMP      LP,#BUFF-4 ;TEST DECREMENT OF LP
491 001014 001401          BEQ      .+4
492 001016 000000          HLT
493 001020 010700          ;NOT DECREMENTED TWO WORDS
494          ;TEST THAT PROPER P.C. IS SAVED
495 001022 012706 010050          MOV      #BUFF,LP          ;LINK POINTER SETUP
496 001026 012767 001036 177000  MOV      #RETC1,RTRAP1    ;RETURN FROM TRAP POINTER
497 001034 104400          TRAP                      ;TRAP ON THIS INSTRUCTION
498 001036 022767 001036 007000  RETC1:  CMP      #.BUFF-4   ;CHECK INCREMENTED P.C.
499 001044 001401          BEQ      .+4
500 001046 000000          HLT                      ;INCORRECT P.C.
501 001050 010700          SCOPE
502          ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
503 001052 010700          SCOPE
504 001054 012706 010050          MOV      #BUFF,LP          ;SET UP
505 001060 012767 001076 176746  MOV      #RETD1,RTRAP1    ;SET UP
506 001066 005067 176704          CLR      CC              ;CLEAR CC AND PRIORITY
507 001072 000257          CCC
508 001074 104400          TRAP                      ;TRAP
509 001076 026727 006744 000000  RETD1:  CMP      BUFF-2,#0   ;TEST THAT OLD STATUS WENT TO STACK
510 001104 001401          BEQ      .+4             ;TEST FOR ALL ZEROS
511 001106 000000          HLT                      ;INCORRECT STATUS
512 001110 010700          SCOPE
513 001112 012706 010050          MOV      #BUFF,LP          ;SET UP
514 001116 012767 001134 176710  MOV      #RETE1,RTRAP1    ;SET UP
515 001124 012767 000357 176644  MOV      #357,CC          ;SET PRIORITY
516 001132 104400          TRAP                      ;SET CC
517 001134 026727 006706 000357  RETE1:  CMP      BUFF-2,#357 ;COMPARES STATUS ON STACK
518 001142 001401          BEQ      .+4             ;TEST FOR ALL ONES
519 001144 000000          HLT                      ;INCORRECT STATUS ON STACK
520          ;TEST THAT "NEW" STATUS IS CORRECT
521 001146 012706 010050          MOV      #BUFF,LP          ;SET UP
522 001152 012767 001166 176654  MOV      #RETF1,RTRAP1    ;SET UP
523 001160 005067 176652          CLR      RTRAP1+2        ;CLEAR FUTURE PRIORITY AND CC
524 001164 104400          TRAP
525 001166 100001          RETF1:  BPL      .+4       ;TEST FOR "C" CLEARED
526 001170 000000          HLT                      ;C NOT CLEARED
527 001172 001001          BNE      .+4             ;Z NOT CLEARED
528 001174 000000          HLT                      ;Z NOT CLEARED
529 001176 102001          BVC      .+4             ;V NOT CLEARED
530 001200 000000          HLT                      ;V NOT CLEARED
531 001202 103001          BCC      .+4             ;C NOT CLEARED
532 001204 000000          HLT                      ;C NOT CLEARED
533 001206 032767 000340 176562  BIT      #340,CC          ;TEST PRIORITY
534 001214 001401          BEQ      .+4
535 001216 000000          HLT                      ;PRIORITY NOT ZERO
536 001220 010700          SCOPE
537 001222 012706 010050          MOV      #BUFF,LP          ;SET UP
538 001226 012767 001244 176600  MOV      #RETG1,RTRAP1    ;SET NEW "CC" AND PRIORITY
539 001234 012767 000357 176574  MOV      #357,RTRAP1+2   ;TRAP HERE
540 001242 104400          TRAP
  
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# L01

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541 001244 100401          RETG1: BMI      .+4
542 001246 000000          HLT              ;N NOT SET
543 001250 001401          BEQ      .+4
544 001252 000000          HLT              ;Z NOT SET
545 001254 102401          BVS      .+4
546 001256 000000          HLT              ;V NOT SET
547 001260 103401          BCS      .+4
548 001262 000000          HLT              ;C NOT SET
549 001264 016706 176506   MOV      CC,LP
550 001270 042706 000017   BIC      #17,LP
551 001274 022706 000340   CMP      #340,LP
552 001300 001401          BEQ      .+4
553 001302 000000          HLT              ;PRIORITY WAS CHANGED
554 001304 010700          SCOPE
555                                ;TEST THAT ALL COMBINATION OF "TRAP" WILL CAUSE A TRAP
556 001306 012767 104400 000012   MOV      #TRAP,RB1 ;INITIALIZE BASE TRAP INSTRUCTION
557 001314 012767 001332 176512   MOV      #RA1,34 ;RETURN FROM TRAP TO RA1
558 001322 012706 010050          RC1: MOV      #BUFF,LP ;SET UP STACK POINTER
559 001326 104400          RB1: TRAP ;TRAP INST WILL BE MODIFIED TO TRAP +377
560 001330 000000          HLT ;PREVIOUS INST FAILED TO TRAP
561 001332 005267 177770          RA1: INC      RB1 ;INCREMENT TRAP INSTRUCTION
562 001336 022767 104777 177762   CMP      #104777,RB1 ;TRAP+377 TO UPPER LIMIT
563 001344 103366          BHIS     RC1 ;HAVE WE TESTED ALL
564 001346 010700          SCOPE ;YES
565 001350 012767 000036 176456   MOV      #36,34
566 001356 005067 176454          CLR      36
567                                ;TEST THAT A TRAP OCCURS ON AN "IOT" INSTRUCTION
568 001362 010700          SCOPE
569 001364 012706 010050          MOV      #BUFF,LP ;LINK POINTER SETUP
570 001370 012767 001402 176422   MOV      #RETA2,RTRAP2 ;RETURN LOCATION
571 001376 000004          IOT ;RESERVED INSTRUCTION, SHOULD TRAP
572 001400 000000          HLT
573 001402 010700          RETA2: SCOPE
574                                ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
575 001404 012706 010050          MOV      #BUFF,LP ;LINK POINTER SETUP
576 001410 012767 001420 176402   MOV      #RETB2,RTRAP2 ;RETURN POINTER
577 001416 000004          IOT ;RESERVED INSTRUCTION
578 001420 020627 010044          RETB2: CMP      LP,#BUFF-4 ;TEST DECREMENT OF LP
579 001424 001401          BEQ      .+4
580 001426 000000          HLT ;NOT DECREMENTED TWO WORDS
581 001430 010700          SCOPE
582                                ;TEST THAT PROPER P.C. IS SAVED
583 001432 012706 010050          MOV      #BUFF,LP ;LINK POINTER SETUP
584 001436 012767 001446 176354   MOV      #RETC2,RTRAP2 ;RETURN FROM TRAP POINTER
585 001444 000004          IOT ;TRAP ON THIS INSTRUCTION
586 001446 022767 001446 006370   RETC2: CMP      #,BUFF-4 ;CHECK FOR INCREMENTED P.C.
587 001454 001401          BEQ      .+4
588 001456 000000          HLT ;INCORRECT P.C.
589 001460 010700          SCOPE
590                                ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
591 001462 010700          SCOPE
592 001464 012706 010050          MOV      #BUFF,LP ;SET UP
593 001470 012767 001506 176322   MOV      #RETD2,RTRAP2 ;SET UP
594 001476 005067 176274          CLR      CC ;CLEAR CC AND PRIORITY
595 001502 000257          CCC
596 001504 000004          IOT ;TRAP

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# M01

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597	001506	026727	006334	000000	RETD2:	CMP	BUFF-2, #0	; TEST THAT OLD STATUS WENT TO STACK
598	001514	001401				BEQ	.+4	; TEST FOR ALL ZEROS
599	001516	000000				HLT		; INCORRECT STATUS
600	001520	010700				SCOPE		
601	001522	012706	010050			MOV	#BUFF, LP	; SET UP
602	001526	012767	001546	176264		MOV	#RETE2, RTRAP2	; SET UP
603	001534	012767	000357	176234		MOV	#357, CC	; SET PRIORITY
604	001542	000277				SCC		; SET CC
605	001544	000004				IOT		; TRAP
606	001546	026727	006274	000357	RETE2:	CMP	BUFF-2, #357	; COMPARES STATUS ON STACK
607	001554	001401				BEQ	.+4	; TEST FOR ALL ONES
608	001556	000000				HLT		; INCORRECT STATUS ON STACK
609	001560	010700				SCOPE		
610								; TEST THAT "NEW" STATUS IS CORRECT
611	001562	012706	010050			MOV	#BUFF, LP	
612	001566	012767	001602	176224		MOV	#RETF2, RTRAP2	
613	001574	005067	176222			CLR	RTRAP2+2	; CLEAR FUTURE PRIORITY AND CC
614	001600	000004				IOT		
615	001602	100001			RETF2:	BPL	.+4	; TEST FOR "C" CLEARED
616	001604	000000				HLT		; C NOT CLEARED
617	001606	001001				BNE	.+4	
618	001610	000000				HLT		; Z NOT CLEARED
619	001612	102001				BVC	.+4	; Z NOT CLEARED
620	001614	000000				HLT		; V NOT CLEARED
621	001616	103001				BCC	.+4	
622	001620	000000				HLT		; C NOT CLEARED
623	001622	032767	000340	176146		BIT	#340, CC	; TEST PRIORITY
624	001630	001401				BEQ	.+4	
625	001632	000000				HLT		; PRIORITY NOT ZERO
626	001634	010700				SCOPE		
627	001636	012706	010050			MOV	#BUFF, LP	
628	001642	012767	001660	176150		MOV	#RETG2, RTRAP2	
629	001650	012767	000357	176144		MOV	#357, RTRAP2+2	; SET NEW "CC" AND PRIORITY
630	001656	000004				IOT		; TRAP HERE
631	001660	100401			RETG2:	BMI	.+4	
632	001662	000000				HLT		; N NOT SET
633	001664	001401				BEQ	.+4	
634	001666	000000				HLT		; Z NOT SET
635	001670	102401				BVS	.+4	
636	001672	000000				HLT		; V NOT SET
637	001674	103401				BCS	.+4	
638	001676	000000				HLT		; C NOT SET
639	001700	016706	176072			MOV	CC, LP	
640	001704	042706	000017			BIC	#17, LP	
641	001710	022706	000340			CMP	#340, LP	
642	001714	001401				BEQ	.+4	
643	001716	000000				HLT		; PRIORITY WAS CHANGED
644	001720	010700				SCOPE		
645	001722	012767	000022	176070		MOV	#22, 20	; .+2
646	001730	005067	176066			CLR	22	; HALT
647								; TEST THAT A TRAP OCCURS ON AN EMT RESTRICTED INSTRUCTION
648	001734	010700				SCOPE		
649	001736	012706	010050			MOV	#BUFF, LP	; LINK POINTER SETUP
650	001742	012767	001754	176060		MOV	#RETA3, RTRAP3	; RETURN LOCATION
651	001750	104000				EMT		; RESERVED INSTRUCTION, SHOULD TRAP
652	001752	000000				HLT		

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653 001754 010700          RETA3:  SCOPE
654          ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
655 001756 012706 010050          MOV      #BUFF,LP          ;LINK POINTER SETUP
656 001762 012767 001772 176040          MOV      #RETB3,RTRAP3    ;RETURN POINTER
657 001770 104000          EMT          ;RESERVED INSTRUCTION
658 001772 020627 010044          RETB3:  CMP      LP,#BUFF-4 ;TEST DECREMENT OF LP
659 001776 001401          BEQ      .+4
660 002000 000000          HLT          ;NOT DECREMENTED TWO WORDS
661          ;TEST THAT PROPER P.C IS SAVED
662 002002 012706 010050          MOV      #BUFF,LP          ;LINK POINTER SETUP
663 002006 012767 002016 176014          MOV      #RETC3,RTRAP3    ;RETURN FROM TRAP POINTER
664 002014 104000          EMT          ;TRAP ON THIS INSTRUCTION
665 002016 022767 002016 006020          RETC3:  CMP      #,BUFF-4  ;CHECK FOR INCREMENTED P.C.
666 002024 001401          BEQ      .+4
667 002026 000000          HLT          ;INCORRECT P.C.
668 002030 010700          SCOPE
669          ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
670 002032 010700          SCOPE
671 002034 012706 010050          MOV      #BUFF,LP          ;SET UP
672 002040 012767 002056 175762          MOV      #RETD3,RTRAP3    ;SET UP
673 002046 005067 175724          CLR      CC              ;CLEAR CC AND PRIORITY
674 002052 000257          CCC
675 002054 104000          EMT          ;TRAP
676 002056 026727 005764 000000          RETD3:  CMP      BUFF-2,#0  ;TEST THAT OLD STATUS WENT TO STACK
677 002064 001401          BEQ      .+4            ;TEST FOR ALL ZEROS
678 002066 000000          HLT          ;INCORRECT STATUS
679 002070 010700          SCOPE          ;INCORRECT STATUS
680 002072 012706 010050          MOV      #BUFF,LP          ;SET UP
681 002076 012767 002116 175724          MOV      #RETE3,RTRAP3    ;SET UP
682 002104 012767 000357 175664          MOV      #357,CC          ;SET PRIORITY
683 002112 000277          SCC          ;SET CC
684 002114 104000          EMT          ;TRAP
685 002116 026727 005724 000357          RETE3:  CMP      BUFF-2,#357 ;COMPARES STATUS ON STACK
686 002124 001401          BEQ      .+4            ;TEST FOR ALL ONES
687 002126 000000          HLT          ;INCORRECT STATUS ON STACK
688 002130 010700          SCOPE
689          ;TEST THAT "NEW" STATUS IS CORRECT
690 002132 012706 010050          MOV      #BUFF,LP          ;SET UP
691 002136 012767 002152 175664          MOV      #RETF3,RTRAP3    ;SET UP
692 002144 005067 175662          CLR      RTRAP3+2        ;CLEAR FUTURE PRIORITY AND CC
693 002150 104000          EMT
694 002152 100001          RETF3:  BPL      .+4      ;TEST FOR "C" CLEARED
695 002154 000000          HLT          ;C NOT CLEARED
696 002156 001001          BNE      .+4
697 002160 000000          HLT          ;Z NOT CLEARED
698 002162 102001          BVC      .+4
699 002164 000000          HLT          ;V NOT CLEARED
700 002166 103001          BCC      .+4
701 002170 000000          HLT          ;C NOT CLEARED
702 002172 032767 000340 175576          BIT      #340,CC          ;TEST PRIORITY
703 002200 001401          BEQ      .+4
704 002202 000000          HLT          ;PRIORITY NOT ZERO
705 002204 010700          SCOPE
706 002206 012706 010050          MOV      #BUFF,LP          ;SET UP
707 002212 012767 002230 175610          MOV      #RETG3,RTRAP3    ;SET UP
708 002220 012767 000357 175604          MOV      #357,RTRAP3+2    ;SET NEW "CC" AND PRIORITY

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709
710 002226 104000
711 002230 100401 RETG3: BMI .+4 ;TRAP HERE
712 002232 000000 HLT ;N NOT SET
713 002234 001401 BEQ .+4
714 002236 000000 HLT ;Z NOT SET
715 002240 102401 BVS .+4
716 002242 000000 HLT ;V NOT SET
717 002244 103401 BCS .+4
718 002246 000000 HLT ;C NOT SET
719 002250 016706 175522 MOV CC,LP
720 002254 042706 000017 BIC #17,LP
721 002260 022706 000340 CMP #340,LP
722 002264 001401 BEQ .+4
723 002266 000000 HLT ;PRIORITY WAS CHANGED
724 002270 010700 SCOPE
725 ;TEST THAT ALL COMBINATION OF EMT WILL CAUSE A TRAP
726 002272 010700 SCOPE
727 002274 012767 104000 000012 MOV #EMT, RB ;INITIALIZE BASE EMT INSTRUCTION
728 002302 012767 LJ2320 175520 MOV #RA, 30 ;RETURN FROM TRAP TO RA
729 002310 012706 010050 RC: MOV #BUFF, LP ;SET UP STACK POINTER
730 002314 104000 RB: EMT ;TRAP INST. WILL BE MODIFIED TO EMT+377
731 002316 000000 HLT ;PRVIOUS INST FAILED TO TRAP
732 002320 005267 177770 RA: INC RB ;INCREMENT TRAP INSTRUCTION
733 002324 022767 104377 177762 CMP #104377, RB ;EMT+377 TO EMT?
734 002332 103366 BHIS RC ;HAVE WE TESTED ALL
735 002334 010700 SCOPE ;YES
736 002336 012767 000032 175464 MOV #32, 30 ;/.+
737 002344 005067 175462 CLR 32 ;HALT
738 ;TEST THAT A TRAP OCCURS ON AN "TRACE-TRT" INSTRUCTION
739 002350 010700 SCOPE
740 002352 012706 010050 MOV #BUFF, LP ;LINK POINTER SETUP
741 002356 012767 002370 175430 MOV #RETA4, RTRAP4 ;RETURN LOCATION
742 002364 000003 TRT ;RESERVED INSTRUCTION, SHOULD TRAP
743 002366 000000 HLT
744 002370 010700 RETA4: SCOPE
745 ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
746 002372 012706 010050 MOV #BUFF, LP ;LINK POINTER SETUP
747 002376 012767 002406 175410 MOV #RETB4, RTRAP4 ;RETURN POINTER
748 002404 000003 TRT ;RESERVED INSTRUCTION
749 002406 020627 010044 RETB4: CMP LP, #BUFF-4 ;TEST DECREMENT OF LP
750 002412 001401 BEQ .+4
751 002414 000000 HLT ;NOT DECREMENTED TWO WORDS
752 002416 010700 SCOPE
753 ;TEST THAT PROPER P.C. IS SAVED
754 002420 012706 010050 MOV #BUFF, LP ;LINK POINTER SETUP
755 002424 012767 002434 175362 MOV #RETC4, RTRAP4 ;RETURN FROM TRAP POINTER
756 002432 000003 TRT ;TRAP ON THIS INSTRUCTION
757 002434 022767 002434 005402 RETC4: CMP #, BUFF-4 ;CHECK FOR INCREMENTED P.C.
758 002442 001401 BEQ .+4
759 002444 000000 HLT ;INCORRECT P.C.
760 002446 010700 SCOPE
761 ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
762 002450 010700 SCOPE
763 002452 012706 010050 MOV #BUFF, LP ;SET UP
764 002456 012767 002474 175330 MOV #RETD4, RTRAP4 ;SET UP

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765	002464	005067	175306		CLR	CC		;CLEAR CC AND PRIORITY
766	002470	000257			CCC			
767	002472	000003			TRT			;TRAP
768	002474	026727	005346	000000	RETD4: CMP	BUFF-2, #0		;TEST THAT OLD STATUS WENT TO STACK
769	002502	001401			BEQ	+.4		;TEST FOR ALL ZEROS
770	002504	000000			HLT			;INCORRECT STATUS
771	002506	010700			SCOPE			
772	002510	012706	010050		MOV	#BUFF, LP		;SET UP
773	002514	012767	002534	175272	MOV	#RETF4, RTRAP4		;SET UP
774	002522	012767	000357	175246	MOV	#357, CC		;SET PRIORITY
775	002530	000277			SCC			;SET-SET CC
776	002532	000003			TRT			;TRAP
777	002534	026727	005306	000357	RETE4: CMP	BUFF-2, #357		;COMPARES STATUS ON STACK
778	002542	001401			BEQ	+.4		;TEST FOR ALL ONES
779	002544	000000			HLT			;INCORRECT STATUS ON STACK
780	002546	010700			SCOPE			
781								;TEST THAT "NEW" STATUS IS CORRECT
782	002550	012706	010050		MOV	#BUFF, LP		
783	002554	012767	002570	175232	MOV	#RETF4, RTRAP4		
784	002562	000003	175230		CLR	RTRAP4+2		;CLEAR FUTURE PRIORITY AND CC
785	002566	000003			TRT			
786	002570	100001			RETF4: BPL	+.4		;TEST FOR "C" CLEARED
787	002572	000000			HLT			;C NOT CLEARED
788	002574	001001			BNE	+.4		
789	002576	000000			HLT			;Z NOT CLEARED
790	002600	102001			BVC	+.4		
791	002602	000000			HLT			;V NOT CLEARED
792	002604	103001			BCC	+.4		
793	002606	000000			HLT			;C NOT CLEARED
794	002610	032767	000340	175160	BIT	#340, CC		;TEST PRIORITY
795	002616	001401			BEQ	+.4		
796	002620	000000			HLT			;PRIORITY NOT ZERO
797	002622	010700			SCOPE			
798	002624	012706	010050		MOV	#BUFF, LP		
799	002630	012767	002646	175156	MOV	#RETF4, RTRAP4		
800	002636	012767	000357	175152	MOV	#357, RTRAP4+2		;SET NEW "CC" AND PRIORITY
801	002644	000003			TRT			;TRAP HERE
802	002646	000401			RETF4: BMI	+.4		
803	002650	000000			HLT			;N NOT SET
804	002652	001401			BEQ	+.4		
805	002654	000000			HLT			;Z NOT SET
806	002656	102401			BVS	+.4		
807	002660	000000			HLT			;V NOT SET
808	002662	103401			BCS	+.4		
809	002664	000000			HLT			;C NOT SET
810	002666	016706	175104		MOV	CC, LP		
811	002672	042706	000017		BIC	#17, LP		
812	002676	022706	000340		CMP	#340, LP		
813	002702	001401			BEQ	+.4		
814	002704	000000			HLT			;PRIORITY WAS CHANGED
815	002706	010700			SCOPE			
816	002710	012767	000016	175076	MOV	#16, 14		
817	002716	005067	175074		CLR	16		
818								;PDP-11 ILLEGAL AND ADDRESS INSTRUCTION TEST
819								;ALL INSTRUCTIONS THAT ARE RESERVED
820								;SHOULD TRAP TO LOCATION 4, AND THE



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821          ;PC THAT POINTS TO THE TRAPPING INSTRUCTION
822          ;SHOULD BE PLACED ON THE STACK
823
824          ;TEST THAT A TRAP OCCURS ON AN ILLEGAL INSTRUCTION
825 002722 010700          SCOPE
826 002724 012706 010050  MOV      #BUFF,LP          ;LINK POINTER SETUP
827 002730 012767 002742 175046  MOV      #RETAS,RTRAPS      ;RETURN LOCATION
828 002736 000100          JMP      %0                ;ILLEGAL INSTRUCTION, SHOULD TRAP
829 002740 000000          HLT
830 002742 010700  RETAS:  SCOPE
831          ;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
832 002744 012706 010050  MOV      #BUFF,LP          ;LINK POINTER SETUP
833 002750 012767 002760 175026  MOV      #RETB5,RTRAPS     ;RETURN POINTER
834 002756 000100          JMP      %0                ;RESERVED INSTRUCTION
835 002760 020627 010044  RETB5:  CMP      LP,#BUFF-4  ;TEST DECREMENT OF LP
836 002764 001401          BEQ      .+4
837 002766 000000          HLT          ;NOT DECREMENTED TWO WORDS
838 002770 010700          SCOPE
839          ;TEST THAT PROPER P.C. IS SAVED
840 002772 012706 010050  MOV      #BUFF,LP          ;LINK POINTER SETUP
841 002776 012767 003006 175000  MOV      #RETC5,RTRAPS     ;RETURN FROM TRAP POINTER
842 003004 000100          JMP      %0                ;TRAP ON THIS INSTRUCTION
843 003006 022767 003006 005030  RETC5:  CMP      #.#,BUFF-4  ;CHECK FOR INCREMENTED P.C.
844 003014 001401          BEQ      .+4
845 003016 000000          HLT          ;INCORRECT P.C.
846 003020 010700          SCOPE
847          ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
848 003022 010700          SCOPE
849 003024 012706 010050  MOV      #BUFF,LP          ;SET UP
850 003030 012767 003046 174746  MOV      #RETD5,RTRAPS     ;SET UP
851 003036 005067 174734          CLR      CC                ;CLEAR CC AND PRIORITY
852 003042 000257          CCC
853 003044 000100          JMP      %0                ;TRAP
854 003046 026727 004774 000000  RETD5:  CMP      BUFF-2,#0    ;TEST THAT OLD STATUS WENT TO STACK
855 003054 001401          BEQ      .+4                ;TEST FOR ALL ZEROS
856 003056 000000          HLT          ;INCORRECT STATUS
857 003060 010700          SCOPE
858 003062 012706 010050  MOV      #BUFF,LP          ;SET UP
859 003066 012767 003106 174710  MOV      #RETE5,RTRAPS     ;SET UP
860 003074 012767 000357 174674  MOV      #357,CC           ;SET PRIORITY
861 003102 000277          SCC                ;SET CC
862 003104 000100          JMP      %0                ;TRAP
863 003106 026727 004734 000357  RETE5:  CMP      BUFF-2,#357  ;COMPARES STATUS ON STACK
864 003114 001401          BEQ      .+4                ;TEST FOR ALL ONES
865 003116 000000          HLT          ;INCORRECT STATUS ON STACK
866 003120 010700          SCOPE
867          ;TEST THAT "NEW" STATUS IS CORRECT
868 003122 012706 010050  MOV      #BUFF,LP          ;SET UP
869 003126 012767 003142 174650  MOV      #RETF5,RTRAPS     ;SET UP
870 003134 005067 174646          CLR      RTRAPS+2         ;CLEAR FUTURE PRIORITY AND CC
871 003140 000100          JMP      %0                ;TEST FOR "C" CLEARED
872 003142 100001  RETF5:  BPL      .+4                ;C NOT CLEARED
873 003144 000000          HLT
874 003146 001001          BNE      .+4
875 003150 000000          HLT          ;Z NOT CLEARED
876 003152 102001          BVC      .+4

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877	003154	000000			HLT				;V NOT CLEARED
878	003156	103001			BCC	.+4			
879	003160	000000			HLT				;C NOT CLEARED
880	003162	032767	000357	174606	BIT	#357,CC			;TEST PRIORITY
881	003170	001401			BEQ	.+4			
882	003172	000000			HLT				;PRIORITY NOT ZERO
883	003174	010700			SCOPE				
884	003176	012706	010050		MOV	#BUFF,LP			
885	003202	012767	003220	174574	MOV	#RETS,RTRAPS			
886	003210	012767	000357	174570	MOV	#357,RTRAPS+2			;SET NEW "CC" AND PRIORITY
887	003216	000100			JMP	%0			;TRAP HERE
888	003220	100401			RETS: BMI	.+4			
889	003222	000000			HLT				;N NOT SET
890	003224	001401			BEQ	.+4			
891	003226	000000			HLT				;Z NOT SET
892	003230	102401			BVS	.+4			
893	003232	000000			HLT				;V NOT SET
894	003234	103401			BCS	.+4			
895	003236	000000			HLT				;C NOT SET
896	003240	016706	174532		MOV	CC,LP			
897	003244	022706	000357		CMP	#357,LP			
898	003250	001401			BEQ	.+4			
899	003252	000000			HLT				;PRIORITY WAS CHANGED
900									;TEST THAT A TRAP OCCURS ON ALL ILLEGAL INSTRUCTION
901	003254	010700			SCOPE				
902	003256	012706	010050		MOV	#BUFF,LP			;LINK POINTER SETUP
903	003262	012767	003274	174514	MOV	#RETS,RTRAPS			;RETURN POINTER
904	003270	004000			JSR	%0,%0			;RESERVED INSTRUCTION
905	003272	000000			HLT				
906	003274	010700			RETS: SCOPE				
907									;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION
908	003276	012706	010050		MOV	#BUFF,LP			
909	003302	012767	003312	174474	MOV	#RETJ,RTRAPS			
910	003310	004000			JSR	%0,%0			
911	003312	020627	010044		RETJ: CMP	LP,#BUFF-4			;TEST DECREMENT OF LP
912	003316	001401			BEQ	.+4			
913	003320	000000			HLT				;NOT DECREMENTED TWO WORDS
914	003322	010700			SCOPE				
915									;TEST THAT PROPER P.C. IS SAVED
916	003324	012706	010050		MOV	#BUFF,LP			;LINK POINTER SETUP
917	003330	012767	003340	174446	MOV	#RETK,RTRAPS			;RETURN FROM TRAP POINTER
918	003336	004000			INSTK: JSR	%0,%0			;TRAP ON THIS INSTRUCTION
919	003340	022767	003340	004476	RETK: CMP	#INSTK+2,BUFF-4			;CHECK FOR INCREMENTED P.C.
920	003346	001401			BEQ	.+4			
921	003350	000000			HLT				;INCORRECT P.C.
922	003352	010700			SCOPE				
923									;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
924	003354	010700			SCOPE				
925	003356	012706	010050		MOV	#BUFF,LP			;SET UP
926	003362	012767	003400	174414	MOV	#RETL,RTRAPS			;SET UP
927	003370	005067	174402		CLR	CC			;CLEAR CC AND PRIORITY
928	003374	000257			CCC				
929	003376	004000			JSR	%0,%0			;TRAP
930	003400	026727	004442	000000	RETL: CMP	BUFF-2,%0			;TEST THAT OLD STATUS WENT TO STACK
931	003406	001401			BEQ	.+4			;TEST FOR ALL ZEROS
932	003410	000000			HLT				;INCORRECT STATUS

933	003412	010700			SCOPE		
934	003414	012706	010050		MOV	#BUFF,LP	;SET UP
935	003420	012767	003440	174356	MOV	#RETM,RTRAP5	;SET UP
936	003426	012767	000357	174342	MOV	#357,CC	;SET PRIORITY
937	003434	000277			SCC		;SET CC
938	003436	004000			JSR	%0,%0	;TRAP
939	003440	026727	004402	000357	RETM: CMP	BUFF-2,#357	;COMPARES STATUS ON STACK
940	003446	001401			BEQ	.+4	;TEST FOR ALL ONES
941	003450	000000			HLT		;INCORRECT STATUS ON STACK
942	003452	010700			SCOPE		
943					;TEST THAT "NEW" STATUS IS CORRECT		
944	003454	012706	010050		MOV	#BUFF,LP	
945	003460	012767	003474	174316	MOV	#RETN,RTRAP5	
946	003466	005067	174314		CLR	RTRAP5+2	;CLEAR FUTURE PRIORITY AND CC
947	003472	004000			JSR	%0,%0	
948	003474	100001			RETN: BPL	.+4	;TEST FOR "C" CLEARED
949	003476	000000			HLT		;C NOT CLEARED
950	003500	001001			BNE	.+4	
951	003502	000000			HLT		;Z NOT CLEARED
952	003504	102001			BVC	.+4	
953	003506	000000			HLT		;V NOT CLEARED
954	003510	103001			BCC	.+4	
955	003512	000000			HLT		;C NOT CLEARED
956	003514	016700	174256		MOV	CC,%0	;TEMP STORAGE
957	003520	001401			BEQ	.+4	
958	003522	000000			HLT		;PRIORITY NOT ZERO
959	003524	010700			SCOPE		
960	003526	012706	010050		MOV	#BUFF,LP	
961	003532	012767	003550	174244	MOV	#RETO,RTRAP5	
962	003540	012767	000357	174240	MOV	#357,RTRAP5+2	;SET NEW "CC" AND PRIORITY
963	003546	004000			JSR	%0,%0	;TRAP HERE
964	003550	100401			RETO: BMI	.+4	
965	003552	000000			HLT		;N NOT SET
966	003554	001401			BEQ	.+4	
967	003556	000000			HLT		;Z NOT SET
968	003560	102401			BVS	.+4	
969	003562	000000			HLT		;V NOT SET
970	003564	103401			BCS	.+4	
971	003566	000000			HLT		;C NOT SET
972	003570	016700	174202		MOV	CC,%0	
973	003574	022700	000357		CMP	#357,%0	
974	003600	001401			BEQ	.+4	
975	003602	000000			HLT		;PRIORITY WAS CHANGED
976	003604	010700			SCOPE		
977					;TEST THAT A TRAP OCCURS ON AN ILLEGAL ADDRESS		
978					SCOPE		
979	003606	010700			MOV	#BUFF,LP	;LINK POINTER SETUP
980	003610	012706	010050		MOV	#RETP,RTRAP5	;RETURN LOCATION
981	003614	012767	003630	174162	TST	1	;ILLEGAL ADDRESS INSTRUCTION, SHOULD TRAP
982	003622	005767	174153		HLT		;ILLEGAL ADDRESS DID NOT TRAP
983	003626	000000			RETP: SCOPE		
984	003630	010700			;TEST DECREMENT OF LINK POINTER ON A TRAP OPERATION		
985					MOV	#BUFF,LP	;LINK POINTER SETUP
986	003632	012706	010050		MOV	#RETO,RTRAP5	;RETURN POINTER
987	003636	012767	003650	174140	TST	1	;RESERVED INSTRUCTION
988	003644	005767	174131				

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989 003650 020627 010044      RETQ:  CMP      LP,#BUFF-4      ;TEST DECREMENT OF LP
990 003654 001401              BEQ      .+4
991 003656 000000              HLT
992 003660 010700              SCOPE
993              ;TEST THAT PROPER P.C. IS SAVED
994 003662 012706 010050      MOV      #BUFF,LP      ;LINK POINTER SETUP
995 003666 012767 003700 174110  MOV      #RETR,RTRAPS  ;RETURN FROM TRAP POINTER
996 003674 005767 174101      TST 1      ;TRAP ON THIS INSTRUCTION
997 003700 022767 003700 004136  RETR:  CMP      #.,BUFF-4      ;CHECK FOR INCREMENTED P.C.
998 003706 001401              BEQ      .+4
999 003710 000000              HLT
1000 003712 010700              SCOPE
1001              ;TEST THAT "OLD" CC AND PRIORITY ARE PLACED ON STACK
1002 003714 010700              SCOPE
1003 003716 012706 010050      MOV      #BUFF,LP      ;SET UP
1004 003722 012767 003742 174054  MOV      #RETS,RTRAPS  ;SET UP
1005 003730 005067 174042      CLR      CC            ;CLEAR CC AND PRIORITY
1006 003734 000257              CCC
1007 003736 005767 174037      TST 1      ;TRAP
1008 003742 026727 004100 000000  RETS:  CMP      BUFF-2,#0      ;TEST THAT OLD STATUS WENT TO STACK
1009 003750 001401              BEQ      .+4          ;TEST FOR ALL ZEROS
1010 003752 000000              HLT                ;INCORRECT STATUS
1011 003754 010700              SCOPE
1012 003756 012706 010050      MOV      #BUFF,LP      ;SET UP
1013 003762 012767 004004 174014  MOV      #RETT,RTRAPS  ;SET UP
1014 003770 012767 000357 174000  MOV      #357,CC       ;SET PRIORITY
1015 003776 000277              SCC                ;SET CC
1016 004000 005767 173775      TST 1      ;TRAP
1017 004004 026727 004036 000357  RETT:  CMP      BUFF-2,#357    ;COMPARES STATUS ON STACK
1018 004012 001401              BEQ      .+4          ;TEST FOR ALL ONES
1019 004014 000000              HLT                ;INCORRECT STATUS ON STACK
1020 004016 010700              SCOPE
1021              ;TEST THAT "NEW" STATUS IS CORRECT
1022 004020 012706 010050      MOV      #BUFF,LP      ;SET UP
1023 004024 012767 004042 173752  MOV      #RETU,RTRAPS  ;SET UP
1024 004032 005067 173750      CLR      RTRAPS+2      ;CLEAR FUTURE PRIORITY AND CC
1025 004036 005767 173737      TST 1      ;TRAP HERE
1026 004042 100001      RETU:  BPL      .+4      ;TEST FOR "C" CLEARED
1027 004044 000000              HLT                ;C NOT CLEARED
1028 004046 001001              BNE      .+4
1029 004050 000000              HLT                ;Z NOT CLEARED
1030 004052 102001              BVC      .+4
1031 004054 000000              HLT                ;V NOT CLEARED
1032 004056 103001              BCC      .+4
1033 004060 000000              HLT                ;C NOT CLEARED
1034 004062 032767 000357 173706  BIT      #357,CC       ;TEST PRIORITY FOR ZERO
1035 004070 001401              BEQ      .+4
1036 004072 000000              HLT                ;PRIORITY NOT ZERO
1037 004074 010700              SCOPE
1038 004076 012706 010050      MOV      #BUFF,LP      ;SET NEW "CC" AND PRIORITY
1039 004102 012767 004122 173674  MOV      #RETV,RTRAPS  ;SET UP
1040 004110 012767 000357 173670  MOV      #357,RTRAPS+2 ;TRAP HERE
1041 004116 005767 173657      TST 1
1042 004122 100401      RETV:  BMI      .+4
1043 004124 000000              HLT                ;N NOT SET
1044 004126 001401              BEQ      .+4

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1045 004130 000000          HLT                ;Z NOT SET
1046 004132 102401          BVS                .+4
1047 004134 000000          HLT                ;V NOT SET
1048 004136 103401          BCS                .+4
1049 004140 000000          HLT                ;C NOT SET
1050 004142 016700 173630    MOV                CC,%0
1051 004146 022700 000357    CMP                #357,%0
1052 004152 001401          BEQ                .+4
1053 004154 000000          HLT
1054 004156 010700          SCOPE
1055                                ;TEST THAT BIT 4; 20(8) WILL CAUSE A TRAP TO 14
1056 004160 010700          SCOPE
1057 004162 012706 010050    MOV                #BUFF,LP
1058 004166 012767 004206 173620    MOV                #RETAT,RTRAP4 ;SET UP TO TRAP TO 14
1059 004174 052767 000020 173574    BIS                #20,CC        ;SET TRACE BIT
1060 004202 000240          NOP                ;TRAP HERE
1061 004204 000000          HLT                ;TRACE BIT DOES NOT TRAP
1062 004206 010700          RETAT: SCOPE
1063                                ;TEST LINK POINTER DECREMENTS
1064 004210 012706 010050    MOV                #BUFF,LP
1065 004214 012767 004230 173572    MOV                #RETBT,RTRAP4
1066 004222 052767 000020 173546    BIS                #20,CC
1067 004230 020627 010044    RETBT: CMP          LP,#BUFF-4
1068 004234 001401          BEQ                .+4
1069 004236 000000          HLT
1070 004240 010700          SCOPE                ;STACK POINTER WAS NOT PUSHED BY TRAP
1071                                ;TEST FOR PROPER PC ON STACK
1072 004242 012706 010050    MOV                #BUFF,LP
1073 004246 012767 004264 173540    MOV                #RETCT,RTRAP4
1074 004254 052767 000020 173514    BIS                #20,CC
1075 004262 000240          NOP
1076 004264 022767 004264 003552    RETCT: CMP          #,BUFF-4
1077 004272 001401          BEQ                .+4
1078 004274 000000          HLT                ;CORRECT PC WAS NOT SAVED ON STACK
1079 004276 010700          SCOPE
1080                                ;TEST THAT DECREMENT R6 TO A VALUE LESS THAN 400 TRAPS
1081                                ;R6 = 150
1082 004300 012706 000150    MOV                #150,%6
1083 004304 012767 004316 173472    MOV                #TDEC1,4
1084 004312 005746          TST                -(6)
1085 004314 000000          HLT                ;STACK OVERFLOW TRAP POINTER
1086 004316 010700          TDEC1: SCOPE        ;WITH R6 = 150 SHOULD TRAP
1087                                ;AUTO DECREMENT WITH R6 LESS THAN 400
1088                                ;DID NOT TRAP
1089                                ;TEST FOR DECREMENT OF R6 ON OVERFLOW TRAP
1090 004320 012706 000150    MOV                #150,%6
1091 004324 012767 004334 173452    MOV                #TDEC2,4
1092 004332 005746          TST                -(6)
1093 004334 020627 000142    TDEC2: CMP          %6,#142
1094 004340 001401          BEQ                .+4
1095 004342 000000          HLT                ;R6 NOT = 142
1096 004344 010700          SCOPE
1097                                ;TEST THAT OVERFLOW TRAP DOES NOT LOSE INFORMATION
1098 004346 012706 000150    MOV                #150,%6
1099 004352 005067 173570    CLR                146
1100 004356 012767 004366 173420    MOV                #TDEC3,4
                                ;STATUS WORD OF LOC 10
                                ;RETURN TO LOC 4

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1101 004364 005246          INC      -(6)
1102 004366 005767 173554  TDEC3:  TST      146
1103 004372 001001          BNE      .+4
1104 004374 000000          HLT
                                     ;INCREMENT OPERATION NOT INHIBITED
1105 004376 010700          SCOPE
1106 004400 012705 001000      MOV      #1000,%5
1107 004404 012706 000400      MOV      #400,%6
1108 004410 012767 004422 173366  MOV      #TDEC4,4
1109 004416 124645          CMPB    -(6),-(5)
1110 004420 000000          HLT
                                     ;STACK = 400 AND DECREMENTED, SHOULD TRAP
1111 004422 010700          TDEC4:  SCOPE
1112
1113 004424 012706 000400      MOV      #400,%6
1114 004430 012767 004442 173346  MOV      #TDEC5,4
1115 004436 134546          BITB    -(5),-(6)
1116 004440 000000          HLT
                                     ;NO STACK OVERFLOW TRAP
1117 004442 010700          TDEC5:  SCOPE
1118 004444 000407          BR      TDEC6
1119 004446 010700          TONT:   SCOPE
                                     ;TEST TRAP ON TRAP - SHOULD CAUSE A HALT
1120
1121 004450 005006          CLR      %6
1122 004452 012767 004464 173324  MOV      #TDEC6,4
1123 004460 000146          JMP      -(6)
1124 004462 000000          HLT
                                     ;TRAP ON TRAP SHOULD HALT
1125 004464 010700          TDEC6:  SCOPE
1126          .MACR  VTRP  INST,A,B,DEST
1127          ;TEST THAT AN INST CAUSES AN OVERFLOW TRAP
1128
1129          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1130          MOV      #VDEC'B,DEST    ;SET UP INST VECTOR
1131          MOV      #VDEC'A,4      ;SET UP OVERFLOW VECTOR
1132          INST                    ;THIS TRAP SHOULD CAUSE OVERFLOW
1133          HLT                    ;NO TRAP OCCURRED
1134          VDEC'B':HLT            ;TRAP FLAG OVERFLOW DID NOT OCCUR
1135          VDEC'A':SCOPE          ;NORMAL OVERFLOW RETURN
1136          .ENDM
1137
1138 004466          VTRP  70000,1,2,10
1139          ;TEST THAT AN 70000 CAUSES AN OVERFLOW TRAP
1140
1141 004466 012706 000400      MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1142 004472 012767 004512 173310  MOV      #VDEC2,10        ;SET UP 70000 VECTOR
1143 004500 012767 004514 173276  MOV      #VDEC1,4        ;SET UP OVERFLOW VECTOR
1144 004506 070000          70000                    ;THIS TRAP SHOULD CAUSE OVERFLOW
1145 004510 000000          HLT                    ;NO TRAP OCCURRED
1146 004512 000000          VDEC2:HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR
1147 004514 010700          VDEC1:SCOPE            ;NORMAL OVERFLOW RETURN
1148 004516          VTRP  IOT,3,4,20
1149          ;TEST THAT AN IOT CAUSES AN OVERFLOW TRAP
1150
1151 004516 012706 000400      MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1152 004522 012767 004542 173270  MOV      #VDEC4,20        ;SET UP IOT VECTOR
1153 004530 012767 004544 173246  MOV      #VDEC3,4        ;SET UP OVERFLOW VECTOR
1154 004536 000004          IOT                    ;THIS TRAP SHOULD CAUSE OVERFLOW
1155 004540 000000          HLT                    ;NO TRAP OCCURRED
1156 004542 000000          VDEC4:HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR

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1157 004544 010700          VDEC3:SCOPE          ;NORMAL OVERFLOW RETURN
1158 004546                VTRP      EMT 5,6,30
1159                ;TEST THAT AN EMT CAUSES AN OVERFLOW TRAP
1160
1161 004546 012706 000400          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1162 004552 012767 004572 173250    MOV      #VDEC6,30       ;SET UP EMT VECTOR
1163 004560 012767 004574 173216    MOV      #VDEC5,4        ;SET UP OVERFLOW VECTOR
1164 004566 104000                EMT                    ;THIS TRAP SHOULD CAUSE OVERFLOW
1165 004570 000000                HLT                    ;NO TRAP OCCURRED
1166 004572 000000          VDEC6:HLT                ;TRAP FLAG OVERFLOW DID NOT OCCUR
1167 004574 010700          VDEC5:SCOPE          ;NORMAL OVERFLOW RETURN
1168 004576                VTRP      TRAP,7,8,34
1169                ;TEST THAT AN TRAP CAUSES AN OVERFLOW TRAP
1170
1171 004576 012706 000400          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1172 004602 012767 004622 173224    MOV      #VDEC8,34       ;SET UP TRAP VECTOR
1173 004610 012767 004624 173166    MOV      #VDEC7,4        ;SET UP OVERFLOW VECTOR
1174 004616 104400                TRAP                   ;THIS TRAP SHOULD CAUSE OVERFLOW
1175 004620 000000                HLT                    ;NO TRAP OCCURRED
1176 004622 000000          VDEC8:HLT                ;TRAP FLAG OVERFLOW DID NOT OCCUR
1177 004624 010700          VDEC7:SCOPE          ;NORMAL OVERFLOW RETURN
1178 004626                VTRP      TRT,9,10,14
1179                ;TEST THAT AN TRT CAUSES AN OVERFLOW TRAP
1180
1181 004626 012706 000400          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1182 004632 012767 004652 173154    MOV      #VDEC10,14      ;SET UP TRT VECTOR
1183 004640 012767 004654 173136    MOV      #VDEC9,4        ;SET UP OVERFLOW VECTOR
1184 004646 000003                TRT                    ;THIS TRAP SHOULD CAUSE OVERFLOW
1185 004650 000000                HLT                    ;NO TRAP OCCURRED
1186 004652 000000          VDEC10:HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR
1187 004654 010700          VDEC9:SCOPE          ;NORMAL OVERFLOW RETURN
1188 004656                VTRP      ILLA,12,11,4
1189                ;TEST THAT AN ILLA CAUSES AN OVERFLOW TRAP
1190
1191 004656 012706 000400          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1192 004662 012767 004702 173114    MOV      #VDEC11,4       ;SET UP ILLA VECTOR
1193 004670 012767 004704 173106    MOV      #VDEC12,4       ;SET UP OVERFLOW VECTOR
1194 004676 004700                ILLA                   ;THIS TRAP SHOULD CAUSE OVERFLOW
1195 004700 000000                HLT                    ;NO TRAP OCCURRED
1196 004702 000000          VDEC11:HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR
1197 004704 010700          VDEC12:SCOPE          ;NORMAL OVERFLOW RETURN
1198 004706 020627 000370          CMP      %6,#370        ;STACK PUSHED FOUR WORDS?
1199 004712 001401                BEQ      .+4
1200 004714 000000                HLT                    ;TRAP OVERFLOW DID NOT OCCUR
1201 004716                VTRP      ILLB,14,13,4
1202                ;TEST THAT AN ILLB CAUSES AN OVERFLOW TRAP
1203
1204 004716 012706 000400          MOV      #400,%6          ;SET UP STACK TO OVERFLOW
1205 004722 012767 004742 173054    MOV      #VDEC13,4       ;SET UP ILLB VECTOR
1206 004730 012767 004744 173046    MOV      #VDEC14,4       ;SET UP OVERFLOW VECTOR
1207 004736 000100                ILLB                   ;THIS TRAP SHOULD CAUSE OVERFLOW
1208 004740 000000                HLT                    ;NO TRAP OCCURRED
1209 004742 000000          VDEC13:HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR
1210 004744 010700          VDEC14:SCOPE          ;NORMAL OVERFLOW RETURN
1211
1212                ;TEST FOR FALSE OVERFLOW TRAP
    
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1213                                     ;PROGRAM MAY HAVE RELOADED IF OVERFLOW FAILS
1214
1215 004746 012767 005014 173030      MOV      #FOVER,4      ;SET UP OVERFLOW POINTER
1216 004754 012706 001002              MOV      #1002,%6
1217 004760 005746                      TST      -(6)          ;SHOULD NOT OVERFLOW
1218 004762 012706 002002              MOV      #2002,%6
1219 004766 005746                      TST      -(6)          ;SHOULD NOT OVERFLOW
1220 004770 012706 004002              MOV      #4002,%6
1221 004774 005746                      TST      -(6)          ;SHOULD NOT OVERFLOW
1222 004776 012706 010002              MOV      #10002,%6
1223 005002 005746                      TST      -(6)
1224 005004 012706 020000              MOV      #20000,%6    ;SHOULD NOT OVERFLOW
1225 005010 005746                      TST      -(6)
1226 005012 000401                      BR       .+4
1227 005014 000000      FOVER:  HLT              ;FALSE OVERFLOW OCCURRED
1228 005016 010700              SCOPE                ;CHECK STACK TO FIND WHERE
1229                                     ;TEST THAT A TTY INTERRUPT CAUSES AN OVERFLOW TRAP
1230 005020 012767 000340 172750      MOV      #340,STATUS  ;LOCK OUT INTERRUPT
1231 005026 012706 000400              MOV      #400,%6      ;SET UP STACK TO OVERFLOW
1232 005032 012767 005064 172744      MOV      #TDEC7,4     ;SET UP OVERFLOW TRAP
1233 005040 012767 005062 173016      MOV      #TDEC8,64    ;SET UP INTERRUPT VECTOR
1234 005046 012767 000100 172510      MOV      #100,TTCSR   ;SET INTERRUPT ENABLE
1235 005054 005067 172716              CLR      STATUS       ;ALLOW INTERRUPT TO OCCUR
1236 005060 000000              HLT              ;NO INTERRUPT OCCURRED
1237 005062 000000      TDEC8:  HLT              ;TRAP FLAG OVERFLOW DID NOT OCCUR
1238 005064 005067 172474      TDEC7:  CLR      TTCSR ;CLEAR INTERRUPT ENABLE
1239 005070 010700              SCOPE
1240 005072 012706 010050              MOV      #BUFF,LP     ;SCOPE PROTECTION
1241 005076 012767 000006 172700      MOV      #6,4
1242 005104 005067 172674              CLR      4
1243 005110 012767 006262 172666      MOV      #ATRAP,RTRAP5
1244 005116 000167 000034              JMP      R7TRX        ;GO TO ILLEGAL ADDRESS TEST
1245 005122 012706 010050              MOV      #BUFF,LP     ;SCOPE PROTECTION
1246 005126 012767 000006 172650      MOV      #6,4
1247 005134 005067 172644              CLR      4
1248 005140 012767 006262 172636      MOV      #ATRAP,RTRAP5
1249 005146 000167 000004              JMP      R7TRX        ;GO TO ILLEGAL ADDRESS TEST
1250 005152 000000      MAP:    0
1251 005154 000000      MAPT:   0
1252                                     HERE=0
1253                                     ;DOES THE PROCESSOR TRAP WHEN %7 IS ODD?
1254 005156 010700      R7TRX:  SCOPE
1255 005160 012706 010050              MOV      #BUFF,%6     ;SET UP STACK POINTER
1256 005164 012767 005202 172612      MOV      #R7TR1,4     ;RETURN FROM TRAP
1257 005172 012707 000001              MOV      #1,%7        ;PC EQUALS ONE
1258 005176 000000              HLT
1259 005200 000000              HLT
1260 005202 022767 000001 002634  R7TR1:  CMP      #1,BUFF-4
1261 005210 001401              BEQ      .+4          ;CORRECT PC WAS NOT SAVED ON STACK
1262 005212 000000              HLT
1263
1264 005214 010700              SCOPE
1265 005216 012706 010050              MOV      #BUFF,%6     ;STACK POINTER
1266 005222 012767 005236 172554      MOV      #R7TR2,4
1267 005230 005207              INC      %7           ;PC BECOMES ODD
1268 005232 000000      R7TR2A: HLT

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1269 005234 000000
1270 005236 022767 005233 002600 R7TR2: HLT
1271 005244 001401 CMP #R7TR2A+1,BUFF-4
1272 005246 000000 BEQ .+4 ;CORRECT PC NOT ON STACK
1273 005250 010700 HLT
1274 005252 012706 010050 SCOPE
1275 005256 012767 005270 172520 MOV #BUFF,%6
1276 005264 005307 MOV #R7TR3,4
1277 005266 000000 DEC %7 ;MAKE PC ODD
1278 005270 022767 005265 002546 R7TR3: HLT ;SHOULD TRAP
1279 005276 001401 CMP #.-3,BUFF-4 ;CHECK VALUE OF PC ON STACK
1280 005300 000000 BEQ .+4
1281 HLT ;WRONG VALUE ON STACK
1282 005302 010700 SCOPE
1283 005304 012706 010050 MOV #BUFF,%6
1284 005310 012767 005326 172466 MOV #R7TR4,4
1285 005316 000261 SEC ;CARRY EQUALS A 1
1286 005320 006107 ROL %7 ;PC BECOMES ODD
1287 005322 000000 TR4A: HLT
1288 005324 000000 HLT
1289 005326 022767 012645 002510 R7TR4: CMP #TR4A+TR4A+1,BUFF-4 ;CHECK FOR VALUE ON STACK
1290 005334 001401 BEQ .+4
1291 005336 000000 HLT ;WRONG VALUE ON STACK
1292 005340 012767 000006 172436 MOV #6,4 ;RESET UP A HALT FOR TRAP
1293 ;TEST TRAP ON TRAP
1294 ;TEST THAT TRACE BIT TRAPS ARE INHIBITED ON TRAP INST
1295
1296 005346 010700 SCOPE
1297 005350 012706 010050 MOV #BUFF,%6
1298 005354 012767 005434 172432 MOV #TRACE,14 ;TRACE TRAP
1299 005362 005027 000016 CLR #16 ;
1300 005366 012767 005410 172424 MOV #TONT1,20 ;IOT TRAP
1301 005374 005067 000054 CLR FLAG ;SET ON TRACE TRAP
1302 005400 052767 000020 172370 BIS #20,STATUS ;SET TRACE BIT
1303 005406 000004 IOT ;TRAP, NEW CC HAVE TRACE RESET
1304 005410 100001 TONT1: BPL .+4 ;IF TRACE TRAP OCCURRED WILL BRANCH
1305 005412 000000 HLT ;NO TRACE TRAP AT END OF IOT INST.
1306 005414 010700 SCOPE
1307 005416 012767 000016 172370 MOV #16,14
1308 005424 012767 000022 172366 MOV #22,20
1309 005432 000411 BR FLAG+2
1310 005434 012767 177777 000012 TRACE: MOV #-1,FLAG ;SET FLAG DURING TRACE
1311 005442 005767 000006 TST FLAG
1312 005446 001401 BEQ .+4
1313 005450 000000 HLT ;TRACE TRAP NOT INHIBITED
1314 005452 000002 RTI ;TRAP
1315 005454 000000 FLAG: 0
1316 ;TEST THAT THE TRACE BIT WILL CAUSE A TRAP
1317 005456 010700 SCOPE
1318 005460 012706 010050 MOV #BUFF,%6 ;SET UP STACK POINTER
1319 005464 012767 005510 172322 MOV #TRC1,14 ;TRACE TRAP RETURN
1320 005472 005067 172320 CLR 16
1321 005476 012767 000020 172272 MOV #20,CC ;SET THE T BIT
1322 005504 000240 NOP
1323 005506 000000 HLT
1324 005510 036727 002332 000020 TRC1: BIT BUFF-2,#20 ;CHECK FOR T BIT ON STACK

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M02

1325	005516	001001
1326	005520	000000
1327	005522	010700

BNE .+4  
HLT  
SCOPE

;T BIT NOT SAVED ON STACKED



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1384                                     ;TEST RESET WITH TRACE ON
1385 006026 010700                               SCOPE
1386 006030 012706 010050                       MOV      #BUFF,%6      ;SET STACK
1387 006034 012767 006056 171752               MOV      #RESET2,14    ;SET UP TRACE VECTOR
1388 006042 012767 000020 171726               MOV      #20,STATUS    ;SET T BIT IN STATUS REGISTER
1389 006050 000005                               RESET                      ;SHOULD HAVE NO EFFECT
1390 006052 000005                               RESET                      ;NO EFFECT
1391 006054 000000                               HLT                       ;TRACE TRAP FAILED
1392 006056 005067 171714                       RESET2: CLR      STATUS ;CLEAR TRACK
1393 006062 005067 171730                       CLR      16             ;TRACE STATUS
1394
1395                                     ;TEST THAT WHEN TTY INTERRUPTS IT POPS NEW STATUS
1396 006066 000005                               RESET
1397 006070 012706 010050                       MOV      #BUFF,%6      ;SET UP STACK
1398 006074 012767 006120 171762               MOV      #TTY3,64      ;INTERRUPT VECTOR
1399 006102 005067 171670                       CLR      STATUS        ;DROP PROCESSOR PRIORITY
1400 006106 012767 000357 171752               MOV      #357,66       ;HIGH PRIORITY ON INTERRUPT
1401 006114 005167 171444                       COM      TTCSR          ;SHOULD SET INTERRUPT ENABLE & INTERRUPT
1402 006120 016727 171652 000000 TTY3:  MOV      STATUS,#HERE ;SAVE PROCESSOR STATUS
1403 006126 022767 000357 177770               CMP      #357,-2
1404 006134 001401                               BEQ      .+4
1405 006136 000000                               HLT
1406 006140 000005                               RESET                      ;INTERRUPT DID NOT POP CORRECT STATUS
1407 006142 010700                               SCOPE                      ;CLR INTERRUPT ENABLE
1408 006144 012706 010050                       MOV      #BUFF,%6      ;STACK SET UP
1409 006150 012767 006174 171706               MOV      #TTY4,64      ;INTERRUPT VECTOR
1410 006156 005067 171704                       CLR      66             ;CLR NEW STATUS
1411 006162 012767 000157 171606               MOV      #157,STATUS   ;PROCESSOR STATUS
1412 006170 005167 171370                       COM      TTCSR          ;SET INTERRUPT ENABLE
1413 006174 016727 171576 000000 TTY4:  MOV      STATUS,#HERE ;SAVE NEW STATUS
1414 006202 005767 177772                       TST     .-2
1415 006206 001401                               BEQ      .+4
1416 006210 000000                               HLT
1417 006212 005067 171346                       CLR      TTCSR          ;INTERRUPT DID NOT POP CORRECT STATUS
1418 006216 000167 000010                       JMP      ADALL
1419
1420                                     ;ILLEGAL ADDRESS AND INSTRUCTION TEST FOR PDP11
1421                                     ;THIS ROUTINE TEST THAT NO LEGAL ADDRESS
1422                                     ;TRAPS AND THAT AN ILLEGAL ADDRESS TRAPS TO LOCATION 4:
1423 006222 160002                               TSH:    160002
1424 006224 000000                               TSL:    0
1425 006226 000000                               CORL:   0
1426 006230 020000                               CORH:   20000           ;CHANGE TO 40000 FOR 8K
1427
1428 006232 016700 177770                       ADALL:  MOV      CORL,%0  ;LL OF CORE TO REG ZERO
1429 006236 012767 006262 171540               MOV      #ATRAP,4      ;SET UP ADDRESS TRAP ENTRANCE
1430 006244 012706 010050                       NOR:    MOV      #BUFF,LP
1431 006250 105720                               TSTB   (0)+
1432 006252 020067 177752                       CMP     %0,CORH        ;IF OUT SIDE OF CORE, TRAP TO 4
1433 006256 101772                               BLOS   NOR             ;IS POINTER IN SIDE CORE
1434 006260 000000                               AUTO:   HLT
1435                                     ;RETURN HERE ON AN ADDRESS TRAP
1436 006262 020067 177742                       ATRAP:  CMP     %0,CORH ;SHOULD WE HAVE TRAPPED
1437 006266 101001                               BHI    TRAPB
1438 006270 000000                               AUTO1:  HLT
1439 006272 020067 177724                       TRAPB:  CMP     %0,TSH  ;NO, FALSE ADDRESS TRAP

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1440	006276	001362		BNE	NOR		; SHOULD TRAP, NON EXISTANT CORE
1441							; LOOP PROGRAM
1442	006300	010700		SCOPE			
1443	006302	012767	000006	MOV	#6,4	171474	
1444	006310	005067	171472	CLR	6		
1445				; SPECIAL CASE OF ODD: .EVEN .BYTE AND REGISTER 6			
1446		000000		HERE=0			
1447							
1448	006314	000167	000024	JMP	R6TST		
1449	006320	000000		K1:	0		
1450	006322	000000		K2:	0		
1451	006324	000000		K3:	0		
1452	006326	000000		K4:	0		
1453	006330	000000		K5:	0		
1454	006332	000000		K6:	0		
1455	006334	052525		K7:	052525		
1456	006336	052400		K10:	052400		
1457	006340	000000		K11:	0		
1458	006342	000000		K12:	0		
1459				; TEST AUTO INCREMENT AND DECREMENT OF R6 FOR .WORD AND .BYTES			
1460	006344	005006		R6TST:	CLR	%6	
1461	006346	112667	171426	MOVB	(6)+, HERE		; SIX SHOULD INCREMENT BY TWO
1462	006352	020627	000002	CMP	%6, #2		
1463	006356	001401		BEQ	.+4		
1464	006360	000000		HLT			; R6 DID NOT AUTO INCREMENT BY TWO
1465	006362	010700		SCOPE			
1466							
1467	006364	012706	001000	MOV	#1000, %6		
1468	006370	114627	000000	MOVB	-(6), #HERE		; SHOULD DECREMENT BY TWO
1469	006374	020627	000776	CMP	%6, #776		
1470	006400	001401		BEQ	.+4		
1471	006402	000000		HLT			; R6 DID NOT AUTO DECREMENT BY 2
1472	006404	010700		SCOPE			
1473							
1474	006406	005006		CLR	%6		
1475	006410	112626		MOVB	(6)+, (6)+		; DOUBLOS AUTO INCREMENT OF R6
1476	006412	020627	000004	CMP	%6, #4		
1477	006416	001401		BEQ	.+4		
1478	006420	000000		HLT			; WRONG AUTO INCREMENT OF R6
1479	006422	010700		SCOPE			
1480							
1481	006424	005006		CLR	%6		
1482	006426	005004		CLR	%4		
1483	006430	122624		CMPB	(6)+, (4)+		; TEST INCREMENT OF R6
1484	006432	020627	000002	CMP	%6, #2		
1485	006436	001401		BEQ	.+4		
1486	006440	000000		HLT			; WRONG INCREMENT OF R6
1487	006442	010700		SCOPE			
1488							
1489	006444	005006		CLR	%6		
1490	006446	005004		CLR	%4		
1491	006450	122426		CMPB	(4)+, (6)+		; TEST INCREMENT OF R6
1492	006452	020627	000002	CMP	%6, #2		
1493	006456	001401		BEQ	.+4		
1494	006460	000000		HLT			; WRONG INCREMENT OF R6
1495	006462	010700		SCOPE			

1496									
1497	006464	005006			CLR	%6			
1498	006466	005004			CLR	%4			
1499	006470	122624			CMPB	(6)+, (4)+			;TEST INCREMENT OF R4
1500	006472	020427	000001		CMP	%4, #1			
1501	006476	001401			BEQ	.+4			
1502	006500	000000			HLT				;WRONG INCREMENT OF R4
1503	006502	010700			SCOPE				
1504	006504	005006			CLR	%6			
1505	006506	005004			CLR	%4			
1506	006510	122426			CMPB	(4)+, (6)+			;TEST INCREMENT OF R6
1507	006512	020627	000002		CMP	%6, #2			
1508	006516	001401			BEQ	.+4			
1509	006520	000000			HLT				;WRONG INCREMENT OF R6
1510	006522	010700			SCOPE				
1511									
1512	006524	005006			CLR	%6			
1513	006526	005004			CLR	%4			
1514	006530	122426			CMPB	(4)+, (6)+			;TEST INCREMENT OF R4
1515	006532	020427	000001		CMP	%4, #1			
1516	006536	001401			BEQ	.+4			
1517	006540	000000			HLT				;WRONG INCREMENT OF R4
1518	006542	010700			SCOPE				
1519									
1520	006544	012706	001000		MOV	#1000, %6			
1521	006550	124627	000000		CMPB	-(6), #HERE			;TEST DECREMENT OF R6
1522	006554	022706	000776		CMP	#776, %6			
1523	006560	001401			BEQ	.+4			
1524	006562	000000			HLT				;WRONG DECREMENT OF R6
1525	006564	010700			SCOPE				
1526									;TEST TRANSFER OF .BYTE USING R6
1527	006566	012767	123456	177534	MOV	#123456, K5			
1528	006574	012767	050505	177516	MOV	#050505, K1			
1529	006602	012705	006320		MOV	#K1, %5			; %5=(050505)K1
1530	006606	012706	006330		MOV	#K5, %6			; %6(123456)K5
1531	006612	112625			MOVB	(6)+, (5)+			;LOW .BYTE OF R6 TO R5
1532	006614	022767	050456	177476	CMP	#050456, K1			
1533	006622	001401			BEQ	.+4			
1534	006624	000000			HLT				;FALSE TRANSFER OF .BYTE
1535	006626	010700			SCOPE				
1536									
1537	006630	012767	123456	177472	MOV	#123456, K5			
1538	006636	012767	050505	177454	MOV	#050505, K1			
1539	006644	012705	006320		MOV	#K1, %5			; %5(050505)K1
1540	006650	012706	006332		MOV	#K6, %6			; %6(123456)K5
1541	006654	114625			MOVB	-(6), (5)+			;LOW .BYTE OF R6 TO R5 (DECREMENT)
1542	006656	026727	177436	050456	CMP	K1, #050456			
1543	006664	001401			BEQ	.+4			
1544	006666	000000			HLT				;FALSE R6 .BYTE TRANSFER
1545	006670	010700			SCOPE				
1546									
1547	006672	012767	123456	177420	MOV	#123456, K1			
1548	006700	012767	050505	177422	MOV	#050505, K5			
1549	006706	012705	006320		MOV	#K1, %5			; (123456)
1550	006712	012706	006330		MOV	#K5, %6			; (050505)
1551	006716	112526			MOVB	(5)+, (6)+			;LOW OF R5 TO LOW OF R6

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1552	006720	022767	050456	177402	CMP	#050456,K5	
1553	006726	001401			BEQ	+.4	
1554	006730	000000			HLT		;FALSE R6 .BYTE TRANSFER
1555	006732	010700			SCOPE		
1556							
1557	006734	012767	123456	177356	MOV	#123456,K1	
1558	006742	012767	050505	177360	MOV	#050505,K5	
1559	006750	012705	006321		MOV	#K1+1,%5	;123456
1560	006754	012706	006330		MOV	#K5,%6	;050505
1561	006760	112526			MOVB	(5)+,(6)+	;HIGH OF R5 TO LOW OF R6
1562	006762	026727	177342	050647	CMP	K5,#050647	
1563	006770	001401			BEQ	+.4	
1564	006772	000000			HLT		;FALSE R6 .BYTE TRANSFER
1565	006774	010700			SCOPE		
1566							
1567	006776	012767	123456	177314	MOV	#123456,K1	
1568	007004	012767	050505	177316	MOV	#050505,K5	
1569	007012	012705	006321		MOV	#K1+1,%5	;R5=123456=-ODD ADDRESS
1570	007016	012706	006330		MOV	#K5,%6	;R6=050505=-.EVEN ADDRESS
1571	007022	112625			MOVB	(6)+,(5)+	;LOW OF R6 TO HIGH OF R5
1572	007024	022767	042456	177266	CMP	#042456,K1	
1573	007032	001401			BEQ	+.4	
1574	007034	000000			HLT		;FAILED LOW OF 6 TO HIGH OF 5
1575	007036	010700			SCOPE		
1576							
1577	007040	126767	177270	177267	CMPB	K7,K7+1	;TEST .BYTE OPERATION WITH SEQUENTIAL ODD: .EVEN ADDRESS
1578	007046	001401			BEQ	+.4	;SAME .WORD LOW TO HIGH
1579	007050	000000			HLT		;SHOULD COMPARE LOW TO HIGH
1580	007052	010700			SCOPE		
1581							
1582	007054	126767	177255	177252	CMPB	K7+1,K7	;COMPARE ODD TO .EVEN SAME .WORD
1583	007062	001401			BEQ	+.4	
1584	007064	000000			HLT		;ODD TO .EVEN .BYTE FAILURE
1585	007066	010700			SCOPE		
1586							
1587	007070	126767	177243	177236	CMPB	K10+1,K7	;SEQUENTIAL .BYTES
1588	007076	001401			BEQ	+.4	;DIFFERENT .WORDS
1589	007100	000000			HLT		;ODD TO .EVEN FAILED
1590	007102	010700			SCOPE		
1591							
1592	007104	126767	177226	177220	CMPB	K10,K6	
1593	007112	001401			BEQ	+.4	
1594	007114	000000			HLT		; .EVEN TO EVEN FAILED
1595	007116	010700			SCOPE		
1596							
1597	007120	126767	177211	177211	CMPB	K7+1,K10+1	
1598	007126	001401			BEQ	+.4	
1599	007130	000000			HLT		;ODD TO ODD FAILED
1600	007132	010700			SCOPE		
1601							
1602	007134	126767	177176	177175	CMPB	K10,K10+1	
1603	007142	001001			BNE	+.4	
1604	007144	000000			HLT		;LOW TO HIGH IN SAME .WORD FAILED
1605	007146	010700			SCOPE		
1606							
1607	007150	126767	177163	177160	CMPB	K10+1,K10	

1608	007156	001001			BNE	.+4	
1609	007160	000000			HLT		;HIGH TO LOW IN SAME .WORD FAILED
1610	007162	010700			SCOPE		
1611							
1612	007164	126767	177146	177143	CMPB	K10,K7+1	
1613	007172	001001			BNE	.+4	
1614	007174	000000			HLT		; .EVEN TO ODD FAILED
1615	007176	010700			SCOPE		
1616							
1617							
1618							;TEST SPECIAL CASE [R,(R)+]
1619	007200	012700	006340		MOV	#K11,%0	;SOURCE AND DESTINATION BOTH R0
1620	007204	010020			MOV	%0,(0)+	;SOURCE NO MEMORY REFERENCE
1621	007206	026727	177126	006342	CMP	K11,#K11+2	;DESTINATION IS MEMORY REFERENCE
1622	007214	001402			BEQ	.+6	
1623	007216	000167	000072		JMP	CPU05	;FAILED %(0),(0)+
1624	007222	010700			SCOPE		
1625	007224	012700	006340		MOV	#K11,%0	
1626	007230	110020			MOVB	%0,(0)+	
1627	007232	026727	177102	006341	CMP	K11,#K11+1	
1628	007240	001401			BEQ	.+4	
1629	007242	000000			HLT		;FAILED MOVB %0,(0)+
1630	007244	010700			SCOPE		
1631							
1632	007246	012706	006340		MOV	#K11,%6	
1633	007252	110626			MOVB	%6,(6)+	
1634	007254	026727	177060	006342	CMP	K11,#K11+2	
1635	007262	001401			BEQ	.+4	
1636	007264	000000			HLT		;FAILED MOVB %6,(6)+
1637	007266	010700			SCOPE		
1638							
1639	007270	012706	006340		MOV	#K11,%6	
1640	007274	010626			MOV	%6,(6)+	
1641	007276	026727	177036	006342	CMP	K11,#K11+2	
1642	007304	001401			BEQ	.+4	
1643	007306	000000			HLT		;FAILED MOV %6,(6)+
1644	007310	010700			SCOPE		
1645							
1646	007312	000444			BR	STAND	
1647	007314	012700	006340		MOV	#K11,%0	;SOURCE AND DESTINATION BOTH R0
1648	007320	010020			MOV	%0,(0)+	;SOURCE NO MEMORY REFERENCE
1649	007322	026727	177012	006340	CMP	K11,#K11	;DESTINATION IS MEMORY REFERENCE
1650	007330	001401			BEQ	.+4	
1651	007332	000000			HLT		;FAILED %(0),(0)+
1652	007334	010700			SCOPE		
1653							
1654	007336	012700	006340		MOV	#K11,%0	
1655	007342	110020			MOVB	%0,(0)+	
1656	007344	026727	176770	006340	CMP	K11,#K11	
1657	007352	001401			BEQ	.+4	
1658	007354	000000			HLT		;FAILED MOVB %0,(0)+
1659	007356	010700			SCOPE		
1660							
1661	007360	012706	006340		MOV	#K11,%6	
1662	007364	110626			MOVB	%6,(6)+	
1663	007366	026727	176746	006340	CMP	K11,#K11	



1664	007374	001401			BEQ	.+4	
1665	007376	000000			HLT		;FAILED MOV B %6,(6)+
1666	007400	010700			SCOPE		
1667							
1668	007402	012706	006340		MOV	#K11,%6	
1669	007406	010626			MOV	%6,(6)+	
1670	007410	026727	176724	006340	CMP	K11,#K11	
1671	007416	001401			BEQ	.+4	
1672	007420	000000			HLT		;FAILED MOV %6,(6)+
1673	007422	010700			SCOPE		
1674							
1675	007424	000277			STAND: SCC		;SET STATUS
1676	007426	005067	170344		CLR	STATUS	;CLEAR STATUS
1677	007432	103001			BCC	.+4	
1678	007434	000000			HLT		;C NOT CLEAR
1679	007436	102001			BVC	.+4	
1680	007440	000000			HLT		;V NOT CLEAR
1681	007442	001001			BNE	.+4	
1682	007444	000000			HLT		;Z NOT CLEAR
1683	007446	100001			BPL	.+4	
1684	007450	000000			HLT		;N NOT CLEAR
1685	007452	010700			SCOPE		
1686							
1687	007454	000257			CCC		;CLEAR CONDITION CODES
1688	007456	052767	000017	170312	BIS	#17,STATUS	;SET STATUS TO ONES
1689	007464	103401			BCS	.+4	
1690							
1691	007466	000000			HLT		;C NOT SET
1692	007470	102401			BVS	.+4	
1693	007472	000000			HLT		;V NOT SET
1694	007474	001401			BEQ	.+4	
1695	007476	000000			HLT		;Z NOT SET
1696	007500	100401			BMI	.+4	
1697	007502	000000			HLT		;N NOT SET
1698	007504	010700			SCOPE		
1699							
1700	007506	012700	007700		;TEST THAT ALL	RSERVED INSTRUCTIONS TRAP	
1701	007512	012002			GIN1: MOV	#TABLE,TAB	;TABLE POINTER
1702	007514	012001			MOV	(TAB)+,FIRST	;FIRST OR CURRENT INSTRUCTION
1703	007516	020267	000212		MOV	(TAB)+,LAST	;LAST INSTRUCTION OR GROUP
1704	007522	001413			CMP	FIRST,FINISH	;TESTED ALL
1705	007524	010267	000206		GIN2: BEQ	GIN3	;YES BRANCH
1706	007530	012767	007626	170252	MOV	FIRST,INST	;SET UP INST
1707	007536	012706	010050		MOV	#RET,10	;SET UP RETURN FROM TRAP
1708	007542	005067	170230		MOV	#BUFF,LP	;SET UP LINK POINTER
1709	007546	000167	000164		CLR	CC	;CLEAR PRIORITY
1710	007552	012737	000207	177566	JMP	INST	;EXECUTE RESERVED INSTRUCTION
1711	007560	105737	177564		GIN3: MOV	#207,@#177566	;BELL ON PASS COMPLETE
1712	007564	100375			TSTB	@#177564	
1713	007566	012737	000000	177566	BPL	.-4	;WAIT FOR FLAG
1714	007574	105737	177564		MOV	#0,@#177566	
1715	007600	100375			TSTB	@#177564	
1716	007602	013700	000042		BPL	.-4	
1717	007606	001405			MOV	@#42,%0	
1718	007610	000005			BEQ	DOAGN	
1719	007612	004713			SENDAD: JSR	%7,@%0	

```

1720 007614 000240      NOP
1721 007616 000240      NOP
1722 007620 000240      NOP
1723 007622 000167 170552      DOAGN: JMP      BEGIN      ;LOOP
      :TRAPPING SHOULD SEND YOU HERE
1724      RET:      CMP      LP,#BUFF-4 ;TEST DECREMENT OF LP
1725 007626 020627 010044      BEQ      RET1
1726 007632 001401      HLT
1727 007634 000000      HLT      ;WRONG DECREMENT
1728 007636 026727 000202 007740 RET1:  CMP      BUFF-4,#INST+2 ;LOC OF INST UNINCREMENTED
1729 007644 001401      BEQ      RET2
1730 007646 000000      HLT      ;INST INC ON TRAP
1731 007650 005767 000172      RET2:  TST      BUFF-2
1732 007654 001401      BEQ      .+4
1733 007656 000000      HLT      ;CONDITION CODES SET ON TRAP
1734 007660 005267 000052      INC      INST
1735 007664 005202      INC      FIRST
1736 007666 026701 000044      CMP      INST, LAST
1737 007672 001707      BEQ      GINI
1738 007674 000167 177624      JMP      GIN2      ;SET UP NEW GROUP
1739      TABLE: 6      ;FINISH OLD GROUP
1740 007700 000006      77      ;END OF INSTRUCTION GROUP
1741 007702 000077      210     ;END OF OPERATE
1742 007704 000210      240-1   ;RTS,RT1,JMP
1743 007706 000237      6400
1744 007710 006400      7777
1745 007712 007777      70000
1746 007714 070000      77777
1747 007716 077777      106400
1748 007720 106400      106777
1749 007722 106777      107000
1750 007724 107000      107777
1751 007726 107777      107777
1752 007730 170000      170000
1753 007732 177777      177777
1754 007734 007734      FINISH: .
1755 007736 000000      INST:  HALT
1756 007740 000000      HALT
1757 007742 000000      HALT
1758 007744 000000      HALT
1759 007746 000000      HALT
1760      =.+100
1761 010050 000000      BUFF:  0
1762      000001      .END

```

ADALL	006232	LP	=%000006	RETD2	001506	RTRAP	= 000010	TDEC7	005064
ATRAP	006262	MAP	005152	RETD3	002056	RTRAP1	= 000034	TDEC8	005062
AUTO	006260	MAPT	005154	RETD4	002474	RTRAP2	= 000020	TONT	004446
AUTO1	006270	NOP	= 000240	RETD5	003046	RTRAP3	= 000030	TONT1	005410
BEGIN	000400	NOR	006244	RETE	000564	RTRAP4	= 000014	TRACE	005434
BELL	= 000240	PC	=%000007	RETE1	001134	RTRAP5	= 000004	TRAPA	= 070000
BUFF	010050	RA	002320	RETE2	001546	R0	=%000000	TRAPB	006272
CC	= 177776	RA1	001332	RETE3	002116	R1	=%000001	TACSR	= 177560
CORH	006230	RB	002314	RETE4	002534	R2	=%000002	TRC1	005510
CORL	006226	RB1	001326	RETE5	003106	R3	=%000003	TRC2	005550
CPU05	007314	RC	002310	RETF	000620	R4	=%000004	TRC3	005554
DOAGN	007622	RC1	001322	RETF1	001166	R5	=%000005	TRT	= 000003
FINISH	007734	RESET1	006016	RETF2	001602	R6TST	006344	TR1	005630
FIRST	=%000002	RESET2	006056	RETF3	002152	R7TRX	005156	TR2	005632
FLAG	005454	RET	007626	RETF4	002570	R7TR1	005202	TR3	005712
FOVER	005014	RETA	000420	RETF5	003142	R7TR2	005236	TR4	005716
GIN1	007512	RETAT	004206	RETG	000676	R7TR2A	005232	TR4A	005322
GIN2	007524	RETA1	000772	RETG1	001244	R7TR3	005270	TR5	005714
GIN3	007552	RETA2	001402	RETG2	001660	R7TR4	005326	TSH	006222
HERE	= 000000	RETA3	001754	RETG3	002230	SCOPE	= 010700	TSL	006224
HLT	= 000000	RETA4	002370	RETG4	002646	SP	=%000006	TICSR	= 177564
ILLA	= 004700	RETA5	002742	RETG5	003220	STAND	007424	TTY3	006120
ILLB	= 000100	RETB	000436	RETH5	003274	STATUS	= 177776	TTY4	006174
INST	007736	RETB1	004230	RETJ	003312	ST12K	000270	VDEC1	004514
INSTC	000462	RETB2	001010	RETK	003340	ST16K	000302	VDEC10	004652
INSTK	003336	RETB3	001420	RETL	003400	ST20K	000314	VDEC11	004702
ITRAPS	= 000004	RETB4	001772	RETM	003440	ST24K	000326	VDEC12	004704
K1	006320	RETB5	002406	RETN	003474	ST28K	000340	VDEC13	004742
K10	006336	RETB5	002760	RETO	003550	ST4K	000222	VDEC14	004744
K11	006340	RETC	000464	RETP	003630	ST8K	000256	VDEC2	004512
K12	006342	RETC1	004264	RETQ	003650	TAB	=%000000	VDEC3	004544
K2	006322	RETC2	001036	RETR	003700	TABLE	007700	VDEC4	004542
K3	006324	RETC3	001446	RETS	003742	TDEC1	004316	VDEC5	004574
K4	006326	RETC4	002016	RETT	004004	TDEC2	004334	VDEC6	004572
K5	006330	RETC5	002434	RETU	004042	TDEC3	004366	VDEC7	004624
K6	006332	RETD	000524	RETV	004122	TDEC4	004422	VDEC8	004622
K7	006334	RETD1	001076	RET1	007636	TDEC5	004442	VDEC9	004654
LAST	=%000001			RET2	007650	TDEC6	004464	SENDAD	007612
.	= 010052								

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

\*DZKARA,DZKARZ/SOL/PAGNUM=DZKARA/EN:ABS/LI:ME/DS:ERFZ  
 RUN-TIME: 49.5 SECONDS  
 RUN-TIME RATIO: 94/15=6.0  
 CORE USED: 7K (13 PAGES)

